Parts Standardization Activity Update

Electronic Technology Workshop (ETW) 2017

NASA/Goddard Space Flight Center (GSFC), Greenbelt, Maryland
June 27, 2017

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NASA's Cassini spacecraft about to make one of its dives between Saturn and its innermost rings as part of the mission's grand finale. Cassini will make 22 orbits that swoop between the rings and the planet before ending its mission on Sept. 15, 2017, with a final plunge into Saturn.

Contents

- **Class Y Update**
  - Class Y standard microcircuit drawing **(SMD)**, **qualified** supplier, etc.
- **Partnerships**
  - Activities within NEPAG
  - JC-13, G-11, and G-12
  - A **new Government Working Group (GWG)**
- **Electronic Parts and the Electrostatic Discharge (ESD)**
  - A new major activity, e.g., new JC-13 **Task Group on ESD**
- **Going beyond audits**
  - NASA approach to resolve major issues
  - Solution – Do the homework before submission to Task Group (TG)
    - NASA via Parts Bulletin & ESD surveys
    - DLA through their Engineering Practice (EP) studies
  - Result – Faster resolution of issues by the TG
    - It will help relieve the frequent concern that:
      It takes too long to get anything done!
- **Small Missions, plastic encapsulated microcircuits (PEMs), and others**

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Class Y SMD / Qualification / Certification Status

- **Class Y SMD (Standard Microcircuit Drawing)**
  - DLA generated first SMD draft for a QMLY application specific integrated circuit (ASIC) (see next page)
- **Qualified Manufacturers**
  - Honeywell, Plymouth, MN.
- **Certified Manufacturers**
  - Cobham, Colorado Springs, CO
  - Honeywell, Plymouth, MN
- **Certified Assembly and Test**
  - Kyocera, San Diego, CA
- **Certified Column-Attach Manufacturing**
  - Six Sigma, Milpitas, CA
  - Micross, Crewe, UK
  - BAE Systems, Manassas, VA
- **Recommendation**
  - Develop slash sheets for BME (Base Metal Electrode) IDCs (Inter-Digitized Capacitors) as soon as possible.

Note: **Certification is demonstration of capability to produce a part, and qualification is actually producing the part per the space requirements.**

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First Class Y SMD

REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

Preliminary
Last updated
5/9/17

Class Y SMD

(Class Y Ceramic non hermetic flip chip LGA devices)

REV																		
SHEET																		
REV																		
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33

REV STATUS	REV												
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A	PREPARED BY Phu H. Nguyen	DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 http://www.landandmaritime.dla.mil
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE	CHECKED BY Muhammad A. Akbar	
	APPROVED BY	MICROCIRCUIT, CERAMIC NON HERMETIC FLIP CHIP, DIGITAL, CMOS SOI, GATE ARRAY HX5000, RADIATION HARDENED, MONOLITHIC SILICON
	DRAWING APPROVAL DATE	
AMSC N/A	REVISION LEVEL	SIZE A / CAGE CODE 67268 / 5962-17B01
		SHEET 1 OF XX

DSCC FORM 2233
APR 97

5962-EXXX

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: XX-XX-XX

Approved sources of supply for SMD 5962-17B01 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/default.aspx

Standard microcircuit drawing PIN 1/ 2/	Vendor CAGE number	Vendor similar PIN
5962H17B0106YXC	34168	HX518X
5962H17B0106YYC	34168	HX518Y

1/ Microcircuits devices supplied to this drawing are land grid array (LGA) packages with lead finish mark letter C (gold). However,for future AID drawing column grid array (CGA) or ball grid array (BGA) packages terminal lead finish mark shall be provided with "F".

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
34168	Honeywell Aerospace - Plymouth 12001 Highway 55 Plymouth, MN 55441-4744

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.

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Infusion of New Technology into MIL/Space Standards PIDTP and Its Applicability

- **Issue**
  - How to address the manufacturability, test, quality, and reliability issues unique to new non-traditional assembly/package technologies intended for space applications

- **Solution implemented**
  - A new concept: package integrity demonstration test plan (PIDTP)
  - Each manufacturer shall develop a PIDTP to be approved by the qualifying activity after consultation with the space community.

- **The PIDTP requirement applies to:**
  - Non-hermetic packages
  - Flip-chip assembly
  - Solder terminations
  - (Refer to 38535, Appendix H)

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Infusion of the New Class (Y) Technology into the QML System for Space

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Task Group Activities

- ☑ Review M. Sampson Idea
- ☑ Class Y Concept Development
- ☑ EP Study (DLA-VA)
- ☑ Coordination Meeting at DLA Land & Maritime (April 2012)
- ☑ DLA-VA to update 38535 with Class Y requirements and release the draft version (rev. K) for comments
- ☑ DLA-VQ to begin preparation for auditing Class Y suppliers
- ☑ 38535K Coordination Meeting
- ☑ DLA-VA to date 38535K
- DLA-VQ to begin audit of suppliers to Class Y requirements (in progress)
- Manufacturer Cert and Qual to QML-Y (DLA-VQ) (in progress)
- Users to procure QML-Y flight parts from certified/qualified suppliers (in progress)

Task Group Inputs

Government | Manufacturers | Primes | Others

G-12 Class Y Task Group Non-Hermetics in Space

- ☑ Aeroflex (October 2011)
- ☑ Xilinx (February 2012)
- ☑ Honeywell (May 2012)
- ☑ BAE (October 2012)
- ☑ e2v (January 2013)

Supplier PIDTP Presentation

- ☑ Minnowbrook Conference Oct. 2013, New York
- ☑ CMSE (Feb. 2013), LA

Conference

Task groups with Class Y interest formed and closed out.

Accomplishments to date as of June 5, 2017

- Class Y First SMD Draft
- Qualified Manufacturer – Honeywell
- Certified Manufacturers – Cobham and Honeywell
- Certified Assembly and Test – Kyocera
- Certified Column Attach Manufacturing – Six Sigma, Micross, and BAE
- Recommendation: Develop Slash Sheets for BME IDCs as soon as possible

Note: Certification = Capability Demonstration
Qualification = Actually Producing the Part

BGA / CGA = Ball-Grid Array / Column-Grid Array
BME = Base Metal Electrode
IDC = Inter Digitized Capacitor

PIDTP = Package Integrity Demonstration Test Plan
SMD = Standard Microcircuit Drawing

Partnering

JEDEC JC-13 (Manufacturers)

JC-13	Solid State Devices for Government Products
JC-13.1	Discrete Semiconductors for Government Products
JC-13.2	Microelectronics for Government Products
JC-13.4	Radiation Hardness
JC-13.5	Hybrids and MCMs for Government Products
JC-13.7	New Electronic Device Insertion for Government Products

Joint meeting held 3 times a year

SSTC G-11/G-12 (Industry Users, Primes, Subs)

SAE SSTC G-11	Users of Passive Components
SAE SSTC G-12	Users of Solid State Devices **G-12 Management:** **Chair – A. Touw** **Vice Chair – S. Agarwal**
SAE SSTC G-11 & G-12	Space Subcommittee Chair – S. Agarwal

NASA Centers:

ARC
GRC
GSFC
JPL
JSC
KSC
LaRC
MSFC

Weekly Telecons

Partners from Outside NASA:

U.S. Air Force, U.S. Navy,
U.S. Army, DLA,
The Aerospace Corp,
JHU/APL, ESA, JAXA, CSA

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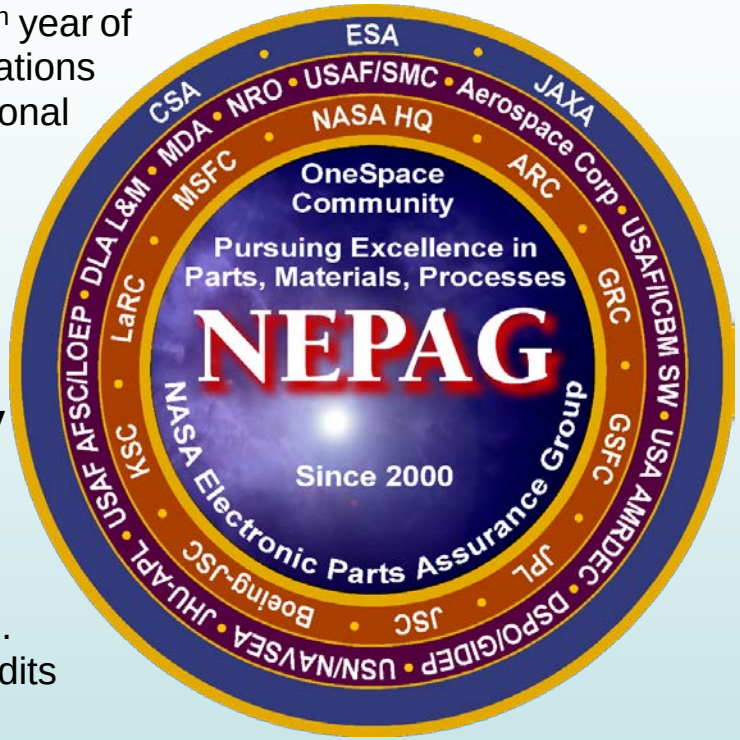
NEPAG Activities

- **Weekly Telecons Drive the NEPAG Program**
  - A forum for exchange of information on electronic parts used on flight projects across NASA (OneNASA) and the space parts community (OneSpace). In its 17th year of operation, NEPAG is comprised of 25 organizations including 7 NASA centers, JPL and 3 international partners from Europe, Japan, and Canada (ESA, JAXA, CSA, respectively).



- **Support to Defense Logistics Agency (DLA) – Audits, SMD Reviews**
  - The Defense Logistics Agency (DLA), the Aerospace Corporation, and NASA form the space microcircuits qualifying activity (QA). Therefore, NASA is actively involved in the audits and standards activities.
  - Audits: VQ is the audits branch of DLA. NASA supports about 25% of the DLA audits. NASA leads audit teams in areas such as burn-in and electrical test program reviews.
  - Standard Microcircuit Drawings (SMDs): VA is the standards/documentation branch of DLA. NASA reviews SMDs for new space products. The SMD program is going strong with about 18–20 new space SMDs created every year.

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JEDEC/G-11/G-12 Schedule (May 2017)

Colorado Springs, CO

FINAL
Meeting Schedule

May 2017

NEPAG MTG.

Day	Room	7:30 AM	8:00 AM	9:00 AM	10:00 AM	11:00 AM	12:00 PM	1:00 PM	2:00 PM	3:00 PM	4:00 PM	5:00 PM	6 PM	7PM
Mon 5/15	Heritage AB							G-12 Derating	JC-13 TM1014 Leak Rate Definitions	G-12 PEM TG Qual and Screening Flow	G-12 Plastics / PEMS Subcommittee	G-12 Terrestrial & Avionics Subcommittee		
	Heritage C							JC-13.1 Technical 750 Test Method Review		JC-13.1 should attend PEMs Screening flow	MIL-PRF-19500R			
	Heriage D						JC-13 ExCo Mtg. (by invitation) *	JC-13.5 TG158 - Element Evaluation		JC-13 TG 17-01 TM 2020				
Day		7:30 AM	8:00 AM	9:00 AM	10:00 AM	11:00 AM	12:00 PM	1:00 PM	2:00 PM	3:00 PM	4:00 PM	5:00 PM	6 PM	7PM
Tues 5/16	Heritage AB	New Member Orientation	JC-13.1/JC-13.7/G-12 New Technology Appendix in 19500	JC-13.1 GaN Working Group	JC-13.1/JC-13.7/G-12 SIC Tech Insertion	JC-13.7 Copper Wire Bonds		JC-13/G-12 Joint Meeting (1-2:30)		JC-13.2 Elec Parameters & B/I Stand. (2:30-3:30)	JC-13 TG 15-02 X-Ray Seal Voids (3:30-4:30)	JC-13 TG 17-03 ESD (4:30-5:30) **	G-12 & G-11 Counterfeit Mitigation Subcommittee	
	Heritage C					JC-13.1 should attend copper wire bond			JC-13.1 MIL-PRF-19500 Appendix J					
	Carson		JC-13 TG 17-02 MIL-STD-883 Inspection and Criteria		JC-13.2 JEP121	JC-13.5 TG 175 - PL / QML			JC-13.5 TG 172 QML Req					
	Summit III		JC-13.4 Subcommittee Meeting						JC-13.4 Extended Session	ASTM				
Day		7:30 AM	8:00 AM	9:00 AM	10:00 AM	11:00 AM	12:00 PM	1:00 PM	2:00 PM	3:00 PM	4:00 PM	5:00 PM	6PM	7PM
Wed 5/17	Heritage AB		G-12 & G-11 1580 DPA Revisions	Joint JC-13.2/G-12 Meeting		Joint JC-13.1/G-12 Meeting		Joint JC-13.7/G-12 New Electronic Device		Joint JC-13.5/G-12 Meeting		G-12 & G-11 Space Subcommittee		
	Heritage C		JC-13.5 Meeting					JC-13.5 Meeting		Chaired by NASA				
	Carson		G-12 Radiation RHA Subcommittee					Joint JC-13.1/JC-13.4 Meeting			Joint JC-13.1/JC-13.4/JC-13.7/G-12/Gan Radiation Effects (3:30-4:30)			
	Heritage EF		G-11 should go to 1580	G-11 Committee Meeting				G-11 Commmittee Meeting						
Day	Room	7:30 AM	8:00 AM	9:00 AM	10:00 AM	11:00 AM	12:00 PM	1:00 PM	2:00 PM	3:00 PM	4:00 PM	5:00 PM	6PM	7PM
Thurs 5/18	Heritage AB		JC-13 General Session		Tech Talk : Die Extraction Process Solution (DER): Replacement Part Manufacturers (RPM)	JC-13 ExCo Meeting (by invitation) *								
	Heritage C		G-11 Committee Meeting											

* Attended by NASA; NASA is G-12 Vice Chair.

** A new JC-13 Task Group on ESD.

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Example SMD Boiler-Plate for a New Requirement

TABLE IIA. Electrical test requirements.

Line Number	Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
		Device class Q	Device class V
1	Interim electrical parameters (see 4.2)	1,2,3,7,8A, 8B,9,10,11 1/	1,2,3,7,8A, 8B,9,10,11 1/
2	Static burn-in I and II (method 1015)	Not required	Required
3	Same as line 1	- - -	1, 7 Δ 1/ 2/
4	Dynamic burn-in (method 1015)	Required	Required
5	Same as line 1	1, 7 Δ 1/ 2/	1, 7 Δ 1/ 2/
6	Final electrical parameters	1,2,3,7,8A,8B,9, 10,11 1/	1,2,3,7,8A,8B,9, 10,11 1/
7	Group A test requirements 3/	1,2,3,4,7,8A,8B,9,10 ,11 4/	1,2,3,4,7,8A,8B,9, 10,11 4/
8	Group C end-point electrical parameters 3/	1,2,3,7,8A,8B, 9,10,11 Δ 2/	1,2,3,7,8A,8B, 9,10,11 Δ 2/
9	Group D end-point electrical parameters 5/	2,3,8A,8B	2,3,8A,8B
10	Group E end-point electrical parameters 3/	1,7,9	1,7,9
11	Column attach 6/	1,7,9	1,7,9

- **For Flip-chip column attach**
  - Add room temperature electricals (subgroups 1, 7, 9) after column attach – step 11 above

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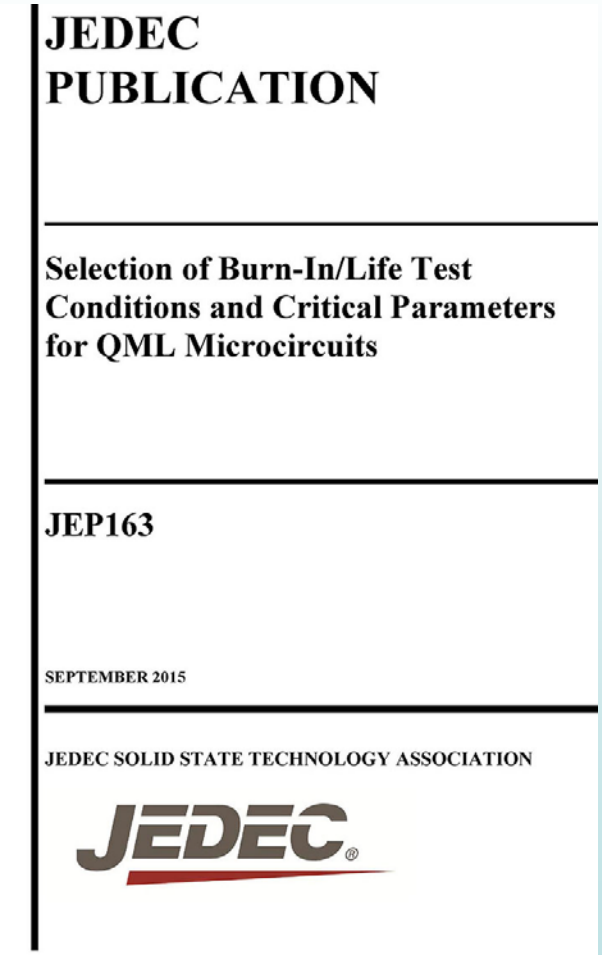
Example of Updated Requirements, Microcircuits Burn-in (BI)
(NASA Inputs 12 September 2016)

- **Status**
  - Task Group until recently was chaired by B. Rhoton. Taken over by N. Shindler going forward.
  - Published Guideline document JEP163.
  - DLA's Engineering Practice (EP) study on BI is complete.
  - Task group is still open to address new concerns

- **A New Concern**
  - BI of high-speed devices (frequencies approaching gigahertz range)
    - What about hot spots on the die? For example, Serializer/Deserializer (SERDES) in a field-programmable gate array (FPGA) may run much hotter than the rest of the die.
      - Practically no data on hot spots (no verification of models)
    - Ambient vs. case vs. junction temperature


JEDEC PUBLICATION

Selection of Burn-In/Life Test Conditions and Critical Parameters for QML Microcircuits

JEP163

SEPTEMBER 2015

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

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Government Meetings

- **Government Working Group (GWG)**
  - Started 2QFY17, weekly telecons to address both space and terrestrial issues
  - Current Participation: NASA, USAF SMC (The Aerospace Corporation), USA AMRDEC, USN NSWC-Crane, USAF Wright-Patterson, and DLA Land and Maritime
- **Some Accomplishments**
  - A one-government response on MIL-STD-883, TM2012 for radiography inspection
  - Comments on MIL-PRF-38534 Revision K
  - Reviewed latest MIL-PRF-32535A draft
  - Reviewed proposal for changes to the QML Class H and Class K periodicity requirements for MIL-PRF-38534
- **Some Topics Currently being Worked**
  - Review of DLA EP Study MIL-STD-981 – lot control for Class S
  - MIL-STD-883K TM2017.12 – Definition of “Crack”
  - Attenuator specifications (e.g., 3933) do not address special marking for use of BeO
  - MIL-PRF-19500 Major Change Definitions

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NEPAG and JEDEC/G-11/G-12

- **FY17 Meetings**
  - Held NEPAG@JEDEC
  - Attended executive committee meetings
  - Chaired Space subcommittee meeting
  - Responsible for G-12 meeting notes
  - Co-lead task group on burn-in
  - Meetings with manufacturers
    - Including State of the Art (SotA)
  - Meetings with OEMs
  - Provide Class Y status report
  - ESD related Support
    - DLA Engineering Practice (EP) Study on electrostatic discharge (ESD)
    - New JC-13 task group on ESD
  - Active participation
    - JC-13.2 (monolithic microcircuits)
    - JC-13.4 (radiation)
    - G-11 (passives)
    - G-12 (actives)
- **Telecons**
  - Plastic encapsulated microcircuits (PEMs) for Space
  - PEMs for Terrestrials/ Avionics
  - JESD 625B and ESDA 20.20 Harmonization

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Other JEDEC/G11/G12 Major Activities Supported by NASA

- Leak rate and residual gas analysis (RGA)
- New technology insertion (>2D packaging)
- GaN, SiC Working Groups
- Hybrid element evaluation
- Passives
- Radiation hardness
- Plastic encapsulated microcircuit (PEM) screening and qual flows
- Copper bond wires qualification, testing
- Other

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Electronic Parts and ESD – NASA Concerns

- **MIL-STD-883, Test Method 3015**
  - Too old
  - Includes only the human body model (HBM)—no mention of the charge device model (CDM),
  - Must be revisited for new technology
    - Smaller feature sizes (down to 45 nm)
    - More contacts/pins (~1750 for Xilinx FPGA)
    - More items; hence, more testing time and touches
    - packaging advances going vertical (2.5D, 3D)
    - **Cumulative result: increased danger of ESD damage**

- **MIL-PRF-38535, Performance Specification for Microcircuits**
  - DLA audits of microcircuit manufacturers and their supply chains
    - Are done to the requirements stated in 38535
  - Poor coverage for ESD
    - No CDM testing required
    - Confusing requirements (e.g., 3 zaps/pin 883 vs. 1 zap/pin for HBM test)
    - No requirements for wafer foundries
    - Many new technologies not covered
    - No requirements for shipping and handling of products in multi-stop supply chain production (which is becoming the norm)
  - **Needs to be updated**

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ESD and Electronic Parts

- **NASA Parts Bulletins**
  - Special edition on ESD
- **Invited Talks**
  - By STS at Space Subcommittee in September 2016
- **DLA Engineering Practice (EP) Study on ESD**
  - DLA presented the results of their EP study in January 2017
- **A New JC-13 Task Group on ESD**
  - JC-13 voted to open a new Task Group on ESD (Chair: P. Coe)
- **JEDEC/ESDA Joint Effort**
  - JESD 625B and S20.20 Harmonization telecons
- **MIL-STD-883, Test Method 1014**
  - Added Para 2.2.1d. "ESD Protective Tubes shall be utilized to ensure the system is ESD safe…"
- **NASA ESD Surveys**

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Electrostatic Discharge

- **NASA EEE Parts Bulletin** (August 2016 – May 2017)

National Aeronautics and Space Administration

EEE Parts Bulletin

Electrical, Electronic, and Electromechanical

A periodic newsletter of the NASA Electronic Parts Program / NASA EEE Parts Assurance Group and the Jet Propulsion Laboratory

August 2016–May 2017 • Volume 9, Issue 1 (Published since 2009), June 16, 2017

Second Special Edition on Electrostatic Discharge (ESD)

Damage from ESD is a major cost to the microcircuit industry in terms of time, money, and mission risk. The first issue dealt with the need to upgrade specifications related to ESD and suggestions for better ESD practices wherever parts are manufactured, stored, or prepared for shipment. This second ESD special issue focuses on a parts failure investigation that ultimately concluded that ESD was the most likely cause of the failure. The issue also includes an important reminder about regular ESD testing and a table of standard microcircuit drawings that were recently reviewed.

Figure 1 is an example of damage that was probably caused by ESD.

Fig. 1. Detailed view of a damaged site on a metal oxide semiconductor field-effect transistor (MOSFET) probably caused by ESD.

ESD, the Silent Killer—

A. Background

There are several great points to consider with respect to ESD knowledge, practice, and compliance. However, the key for ESD program success is consistency. If we detect the results of an event, then, we [the operational group] should be able to ascertain and confirm that we never have any lapses in the program implementation. With systematic practices, we should be able to surmise that there is no way any events can occur on the organizational project watch.

ESD is the silent killer in electronics, and the resulting impacts are hidden project costs that are the motivator to address project risk cost and schedule impacts. When an ESD event occurs, one of three scenarios may play out.

1) There is no impact, and no detrimental result.

2) There is a catastrophic strike and the immediate

1

and shipped off for failure analysis.

Figure 2 shows the PCB assembly with two noted nonfunctional parts circled in red. Although not conclusive, the corner location of damaged parts on the board was thought to be important to the forensics analysis. One theory implied that handling of the board (by the perimeter) allowed for the ESD event to contact these parts directly. During transport, the board is handled only inside an ESD-approved materials bag. There were questions as to the integrity of these transport bags. Due to bag traceability and reuse issues, there was no definite conclusion on this concern.

Figures 3 thru Figure 7 Show the die and damage areas from various photographic and radiographic perspectives. During upper-level assembly circuit troubleshooting, the potential for design or operational damaging voltages to the MOSFET gates were conclusively ruled out. The circuit was incapable of generating the necessary damaging voltages that would have the effect observed.

C. Investigation Conclusion

The conclusion of this ESD failure investigation was that failure was attributed to user error but review of all ESD compliance logs showed that all precautions were taken during operator handling. Due to lack of further evidence, the OCM and the PCB assembly operation were not ruled out as possible culprits, but neither could be confirmed.

Under these circumstances the team was advised of the event and warned of the total cost for repair and the need to double check all future handling procedures. The board was repaired with same lot date code parts, and there were never any repeat operational issues with that PCB assembly nor at the box operational level. The "Silent Killer" only struck once on that program. At least as far as can be determined at this time.

Figures 1 through 7 (provided courtesy of NASA Langley Research Center) were generated by Hi-Rel Labs as part of a project Component Failure Investigation at Langley.

For more information, contact

John E. Pandolf 757 864-9624

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circled in red.

Fig. 3. Optical micrograph of the die in the failed device. The red arrows indicate the damage sites.

damage sites on the die.

Fig. 5. SEM image of one of the damage sites. The arrow indicates the area where the damage originated

ET after delayering. The arrows indicate the damage at the ends of the gate runners.

Fig. 7. SEM image of another damaged area on the die. Note that the gate polysilicon fused during the failure, which is why the oxide is visible.

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NASA Electrostatic Discharge (ESD) Surveys of Microcircuit Manufacturers & Their Supply Chains

- Candidate companies for NASA ESD survey are identified during the DLA audits.
- These are independent surveys by NASA—Not a part of the DLA audit process.
- The purpose of these surveys is to better prepare manufacturers to develop space products.
- The findings of the survey are non-binding.
- There has been good feedback from companies that went through it.

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Growing Complexity/ESD Challenges in Shipping and Handling

A New Trend – Supply Chain Management
Ensuring gap-free alignment for each qualified product
(All entities in the supply chain must be certified/approved)

Manufacturer A	Die design
Manufacturer B	Fabrication
Manufacturer C	Wafer bumping
Manufacturer D	Package design and package manufacturing
Manufacturer E	Assembly
Manufacturer F	Column attach and solderability
Manufacturer G	Screening, electrical and package tests
Manufacturer H	Radiation testing

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How Audits & NASA Surveys Help Expedite Issue Resolution at JEDEC/G12

- **Audits:** NASA, Aerospace Corporation, & other organizations often participate along with the Defense Logistics Agency (DLA) Land & Maritime personnel in DLA audits. DLA audits get better electronic parts by monitoring compliance with the MIL specs & by working with the manufacturers to enhance quality of their products.

- **Surveys:** NASA has conducted electrostatic discharge (ESD) surveys of parts manufacturers. Those surveys produced recommendations regarding ESD mitigation and control. These recommendations are not enforced, but the surveyed companies all implemented the suggestions.

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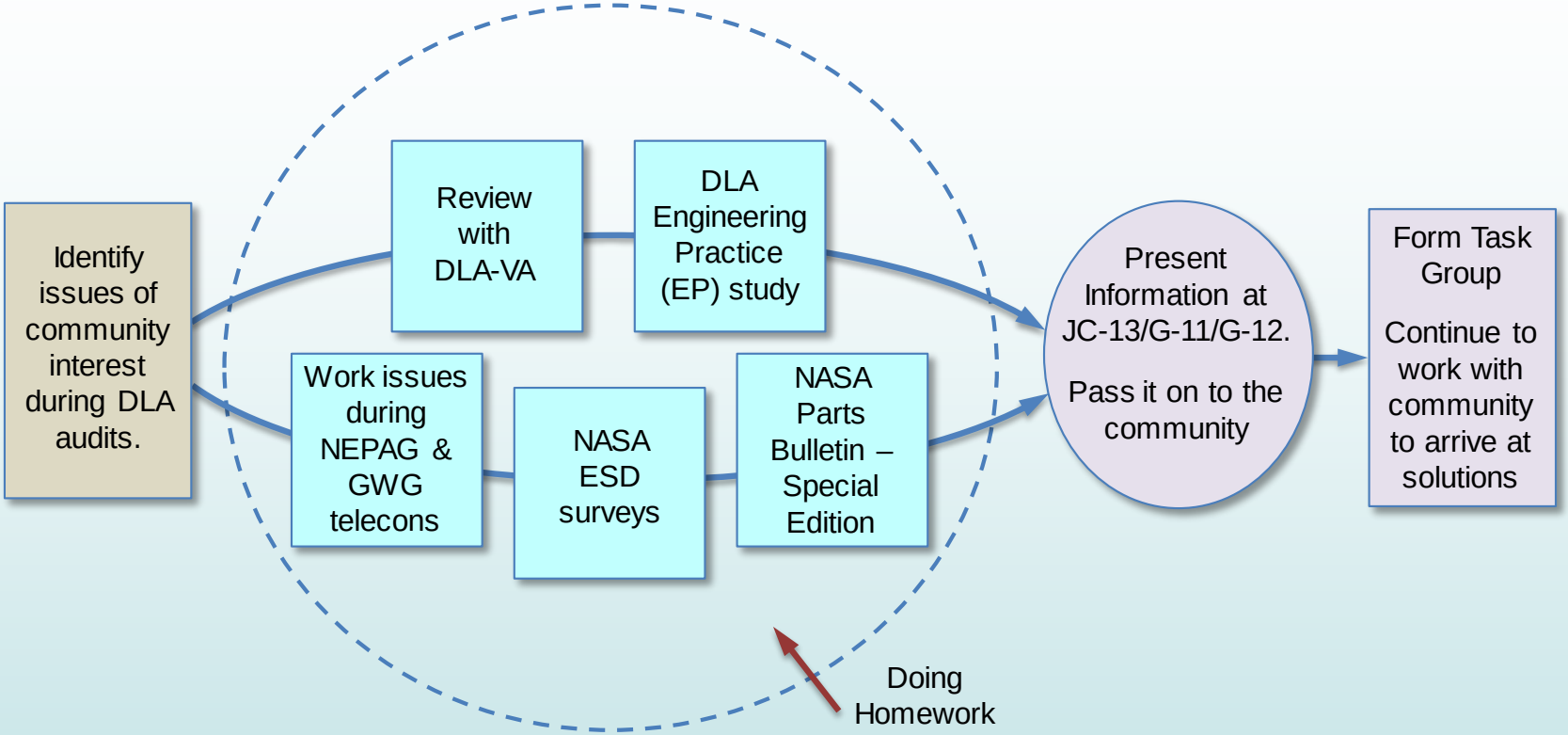
Taking Audit Findings a Step Further!
NASA Timesaving Approach



- Bring general awareness (Via NASA Bulletins, Surveys)
- Work with DLA to help them conduct an engineering practice (EP) study
- Generate a basic proposal and related information so the potential task group (TG) has a strong starting point.
- This path has **saved time** in resolving major issues found during audits.

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Issues from Microcircuit / Other Audits and Methods of Resolution

Audits						
Class Y	New Technology Infusion		NASA Parts Bulletin	DLA Engineering Practice (EP) study	G-12 Task Group (TG)	MIL-PRF-38535 Revision K
Burn-in	Varied interpretations of requirements			DLA Engineering Practice (EP) study	JEDEC Task Group (TG)	JEP163. TG still open
Underfill	Difficulties in meeting requirements		NASA Parts Bulletin – Special Edition on Underfills	DLA Engineering Practice (EP) study	JEDEC Task Group	Resolved
ESD	Old/inconsistent requirements (e.g. 3 zaps vs 1 zap per pin)	NASA ESD Surveys	NASA Parts Bulletin – Special ESD Edition	DLA Engineering Practice (EP) study	DLA presented EP results in January 2017	JC-13 ESD task group formed
Crystal Oscillators	Per manufacturers, practically no sales for QPLS oscillators		NASA Parts Bulletin – in preparation	DLA EP study planned	DLA talk at Space meeting last September	New issue

Process Flow:

*DLA Audits: Major issues uncovered during DLA audits

*NASA Parts Bulletin – Special Edition: Gives subject matter background. Provides results of NASA evaluations, ESD surveys, etc.

*DLA EP Study: A large survey of manufacturers, users, others.

*JEDEC/G11/G12 Meetings: Where discussions are held.

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Growing Use of NASA CubeSats and SmallSats

- **Trend toward CubeSats and SmallSats**
  - Many new NASA flight missions are CubeSats and SmallSats.
  - The weekly NEPAG telecons discuss types of standard products that would fit those applications, including commercial-off-the-shelf (COTS) plastic encapsulated microcircuits (PEMs).

- **Three parts manufacturers are offering customized parts.**
  - Cobham Aeroflex has several flows assigned based on extent of testing to assist users in picking the best parts.
  - Texas Instruments offers parts in five different versions, including their QML offerings.
  - Linear Technology plans to offer PEM products with guaranteed total dose radiation (rad tolerant, RT) ratings.

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Standardized Flows for NASA CubeSats and SmallSats

- **The need for standardization**
  - The developments discussed on previous slide are all good, but
  - It would be cumbersome to manage multiple nonstandard flows.
  - Moreover, some of these approaches may or may not apply to NASA missions depending on acceptable risk levels.

- **Possible methods to get standardized flows**
  - The ideal situation would be for the space community and manufacturers to agree on a limited number of standard QML PEM flows to offer solutions for small missions (CubeSats, NanoSats, SmallSats, etc.).
  - There is an existing QML N flow for standard non-space PEM devices.
  - G12 developed a document SAE AS6294
  - In addition, DLA has Vendor Item Drawing (VID) program and parts built for automotive applications.
  - Of course, every major issue needs to be discussed.

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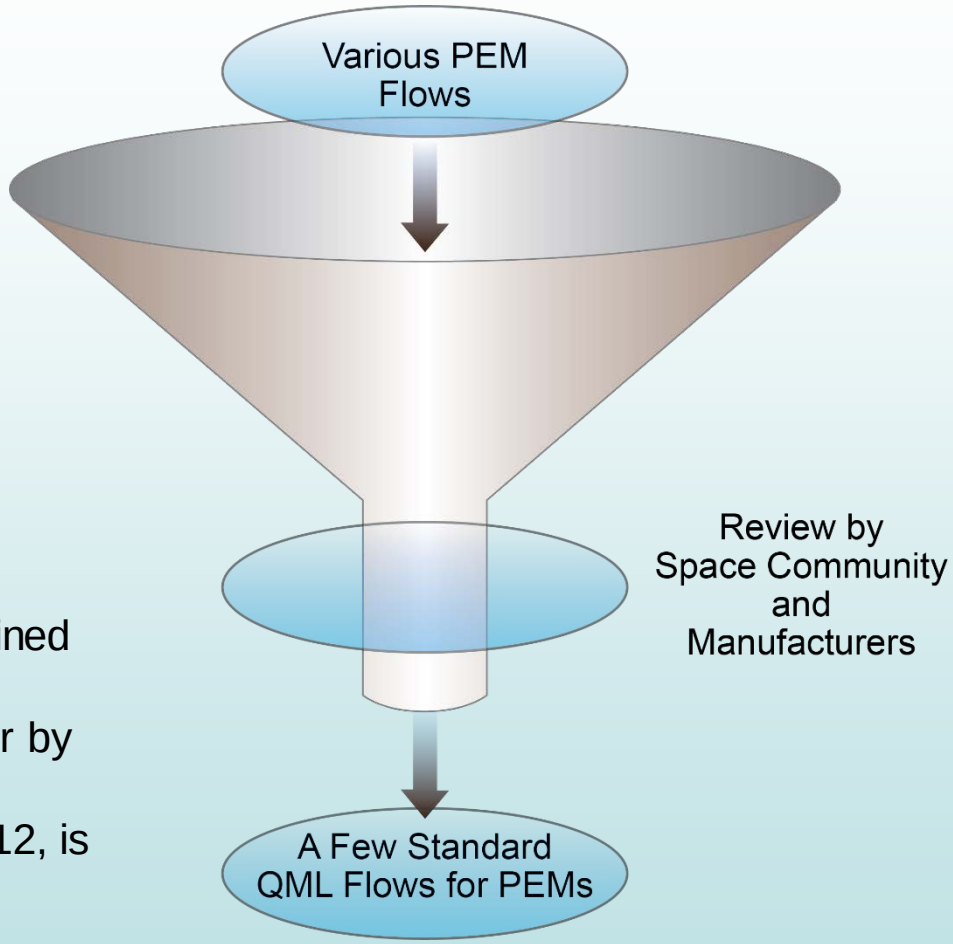
PEMs for Space

- **Newer Applications**
  - CubeSats
  - SmallSats



Standardizing on a few well-defined flows rather than multiple flows defined by each manufacturer or by each standards group.
SAE AS6294, developed by G-12, is one candidate.

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DLA's VID (Vendor Item Drawing) Program

Current Supplier's Program Benefits

1. Single Standardization Document
2. Controlled baseline.
3. Enhanced product change notification of processes, materials, electrical performance, finish, molding compounds and manufacturing locations.
4. Extended temperature performance.
5. Enhanced Pedigree - Reliability and electromigration checks, electrical characterization over temperature and confirmation of package performance over temperature.
6. Enhanced Obsolescence management.
7. No pure tin.
8. No copper wire bonds.

See the attached listing or check our website for an up to date list of product coverage.

DSCC ANNOUNCES THE RELEASE OF A NEW TYPE OF STANDARDIZATION DOCUMENT.

DSCC is releasing new Vendor Item Drawings (VIDs) almost daily. These documents have been created to provide a procurement vehicle for enhanced commercial products. Specifically, commercially available microcircuit products are being documented for the first time on a standardization document. Use of these DSCC VIDs will avoid the use of manufacturer generated specification control drawings (SCDs) or manufacturer's VIDs and avoid the potential proliferation of non-standard products. The participating manufacturers have agreed to provide information and services that have not traditionally been associated with commercial products. See our website for a list of documents that are currently available.

All Vendor Item Drawings are ***NOW*** available on the DSCC web site

http://www.dscc.dla.mil/Programs/MilSpec/

- Analog and digital functions offered.

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Evaluation of Automotive Microcircuits

- **Existing automotive parts market**
  - Plastic packages
  - No screening is done
  - Much testing is done at the wafer level
  - Limited qualification
  - The customer must enforce any desired requirements
  - Manufacturers self certify — no DLA-type regulators
  - The system works because of **high-volume production** — That is the customer's power to enforce upgrades

- **NASA Evaluation is in progress at Navy Crane**
  - Screening and qualification planned
    - Passives, discretes and microcircuits
    - Qualification limited to life test

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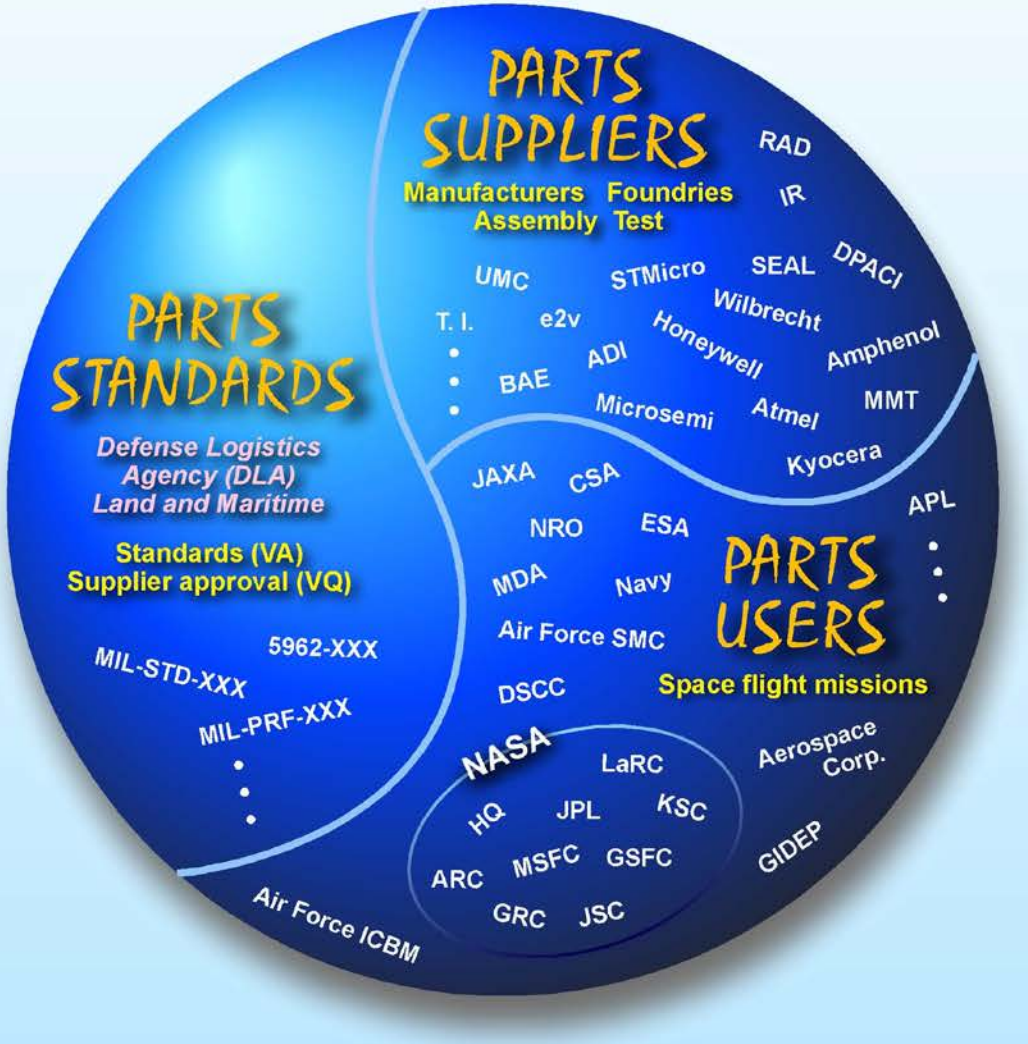
Space Parts World
Develop/Maintain Standards for Space Electronic Parts



The parts users and standards organizations work with suppliers to ensure availability of standard parts for NASA, DoD and others. **For Space microcircuits, DLA, NASA/JPL (S. Agarwal) and the U.S. Air Force / Aerospace Corp. (L. Harzstark) form the Qualifying Activity (QA).**

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NEPP – Charter

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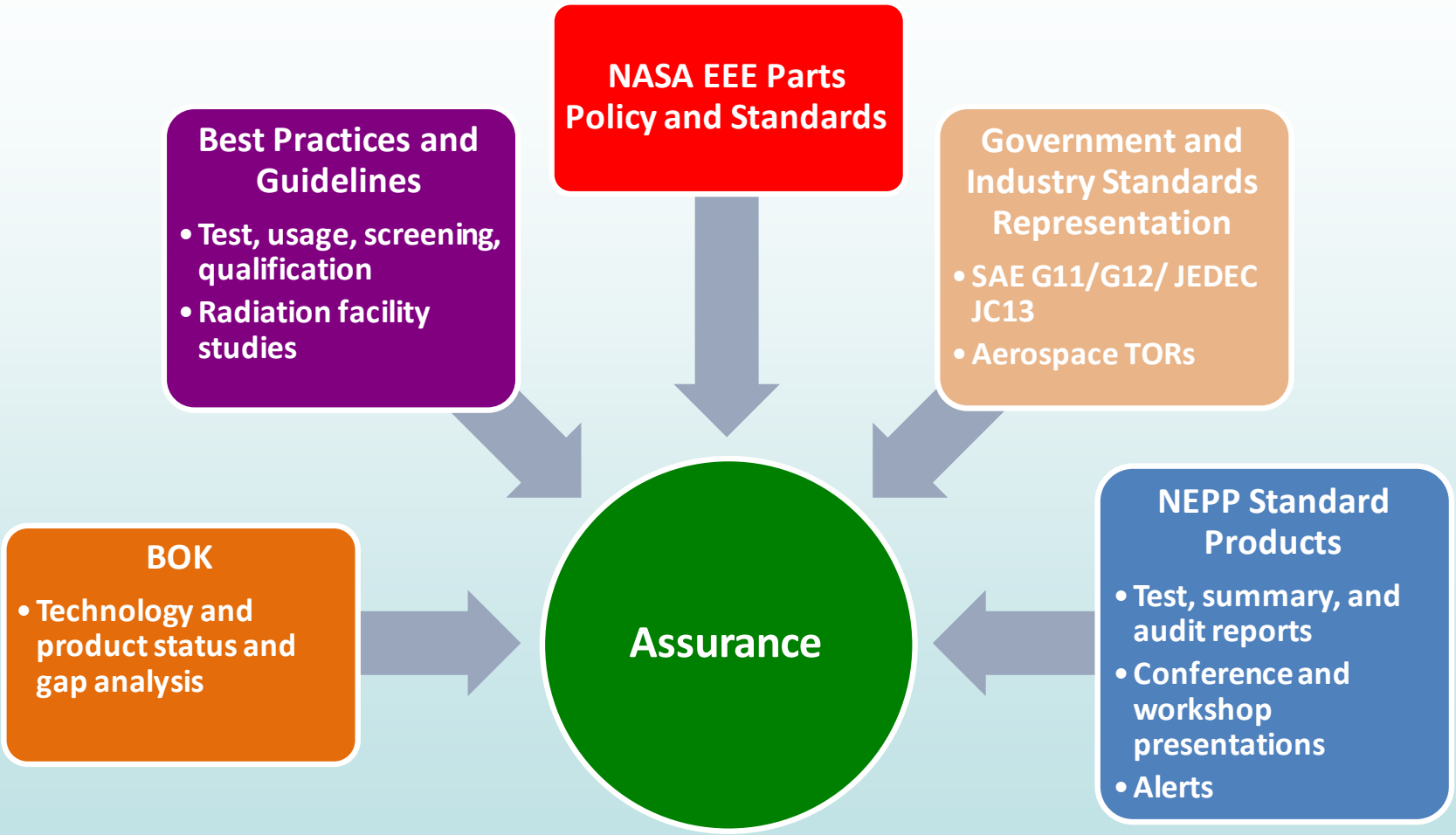
NEPP – Product Delivery



Related task areas:
Technology/parts evaluations lead to new best practices, etc.

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http://nepp.nasa.gov

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